IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Original): An image processing apparatus comprising:

an input terminal for receiving a plurality of color component signals output in parallel from an image sensor;

a plurality of defective pixel correction circuits for correcting said plurality of color component signals associated with a defective pixel of said image sensor with a predetermined timing; and

a defective pixel correction timing generator for generating said predetermined timing used in performing defective pixel correction at a time of input of said plurality of color component signals, wherein

said plurality of defective pixel correction circuits correct said plurality of color component signals in parallel at the same time with said predetermined timing, all of said plurality of color component signals being associated with said defective pixel.

Claim 2 (Original): The image processing apparatus according to claim 1, wherein

said defective pixel correction timing generator generates said predetermined timing based on defect correction data transferred from a memory by a DMA (direct memory access) controller.

Claim 3 (Currently Amended): An image processing apparatus comprising:

[[an]] a plurality of input ~~terminal~~ terminals for receiving a YUV signal and a plurality of color component signals, said YUV signal including a luminance signal and a color difference signal;

a selector for selecting one of said YUV signal and said plurality of color component signals which are input to said selector to provide a plurality of selected signals, and outputting said plurality of selected signals; and

a signal processor for processing said plurality of selected signals, wherein

one of said input ~~terminal~~ terminals is shared by said YUV signal and one of said plurality of color component signals.

Claim 4 (Currently Amended): [[The]] An image processing apparatus ~~according to claim 3, wherein~~ comprising

an input terminal for receiving a YUV signal and a plurality of color component signals, said YUV signal including a luminance signal and a color difference signal;

a selector for selecting one of said YUV signal and said plurality of color component signals which are input to said selector to provide a plurality of selected signals, and outputting said plurality of selected signals; and

a signal processor for processing said plurality of selected signals, wherein

said input terminal is shared by said YUV signal and said plurality of color component signals,

said signal processor comprises:

a plurality of defective pixel correction circuits for correcting said plurality of selected signals associated with a defective pixel of an image sensor with a predetermined timing; and

a defective pixel correction timing generator for generating said predetermined timing used in performing defective pixel correction at a time of input of said plurality of selected signals, and

said plurality of defective pixel correction circuits of said signal processor correct said plurality of selected signals in parallel at the same time with said predetermined timing, all of said plurality of selected signals being associated with said defective pixel.

Claim 5 (Original): The image processing apparatus according to claim 4, further comprising:

an oversampling circuit for interpolating a missing signal using an input signal and outputting a resultant signal to said selector; and

a separation circuit for separating said YUV signal into a plurality of component signals, wherein

said color difference signal included in said YUV signal includes a subsampled color difference signal, and

said oversampling circuit interpolates a missing color difference signal using said subsampled color difference signal output from said separation circuit.

Claim 6 (Original): The image processing apparatus according to claim 5, further comprising

an output control circuit for outputting said YUV signal to a bus without performing any processing on said YUV signal.

Claim 7 (Original): An image processing apparatus comprising:

an input terminal for receiving a multiplex signal output from an image sensor; and

a sampling circuit for sampling said multiplex signal which is input to said sampling circuit, wherein

said multiplex signal is formed by decomposing an N_1-bit (N_1 is a positive integer) wide color component signal into a plurality of N_2-bit (N_2 is a positive integer; N_1 is twice as large as N_2) wide data signals and performing time division multiplexing on said plurality of N_2-bit wide data signals, and

said sampling circuit functions to mix said plurality of N_2-bit wide data signals to convert said plurality of N_2-bit wide data signals into said N_1-bit wide color component signal.

Claim 8 (Original): An image processing apparatus comprising:

an input terminal for receiving a multiplex signal output from an image sensor; and

a sampling circuit for sampling said multiplex signal which is input to said sampling circuit, wherein

said multiplex signal is formed by decomposing an N_1-bit (N_1 is a positive integer) wide color component signal into a plurality of N_2-bit (N_2 is a positive integer; N_1 is three times as large as N_2) wide data signals, and performing time division multiplexing on said plurality of N_2-bit wide data signals, and

said sampling circuit functions to mix said plurality of N_2-bit wide data signals to convert said plurality of N_2-bit wide data signals into said N_1-bit wide color component signal.

Claim 9 (Original): An image processing apparatus comprising:

an input terminal for receiving a multiplex signal output from an image sensor; and

a sampling circuit for sampling said multiplex signal which is input to said sampling circuit, wherein

said multiplex signal is formed by decomposing an N_1-bit (N_1 is a positive integer) wide color component signal into a plurality of N_2-bit (N_2 is a positive integer; N_1 is four times as large as N_2) wide data signals, and performing time division multiplexing on said plurality of N_2-bit wide data signals, and

said sampling circuit functions to mix said plurality of N_2-bit wide data signals to convert said plurality of N_2-bit wide data signals into said N_1-bit wide color component signal.

Claim 10 (Currently Amended): An image processing apparatus comprising[[;]]:

an input terminal for receiving an N_1-bit (N_1 is a positive integer) wide multiplex signal formed by performing time division multiplexing on a plurality of color component signals;

a sampling circuit for sampling said N_1-bit wide multiplex signal input to said sampling circuit to provide said plurality of color component signals, and outputting said plurality of color component signals, as N_2-bit (N_2 is a multiple of N_1) wide signals, in parallel; and

a signal processor for processing said plurality of color component signals output in parallel from said sampling circuit, wherein

said sampling circuit samples said N_1-bit wide multiplex signal to provide said plurality of color component signals using a clock signal at a frequency which is N_2/N_1-times a frequency of a clock signal synchronous with output of said N_2-bit wide signals.

Claim 11 (Original): The image processing apparatus according to claim 10, wherein

said sampling circuit samples said N_1-bit wide multiplex signal to provide said plurality of color component signals using a clock signal at a frequency which is four times

said frequency of said clock signal synchronous with output of said N_2-bit wide signals (N_2 is four times as large as N_1).

Claim 12 (Original): The image processing apparatus according to claim 10, wherein said sampling circuit samples said N_1-bit wide multiplex signal to provide said plurality of color component signals using a clock signal at a frequency which is three times said frequency of said clock signal synchronous with output of said N_2-bit wide signals (N_2 is three times as large as N_1).

Claim 13 (Currently Amended): An image processing system for processing an image signal, comprising:

a signal processor for processing a plurality of image signals in parallel, including phase adjustment in parallel and defective pixel correction in parallel, said plurality of image signals being read out in parallel from a plurality of light receivers of an image sensor;

a plurality of output control circuits for outputting said plurality of image signals which are processed by said signal processor, to a bus, respectively; and

a data transfer controller for transferring said plurality of image signals output to said bus.

Claim 14 (Original): The image processing system according to claim 13, wherein said data transfer controller includes a DMA (direct memory access) controller.

Claim 15 (Currently Amended): ~~The image processing system according to claim 14~~ An image processing system for processing an image signal, comprising:

a signal processor for processing a plurality of image signals in parallel, said plurality of image signals being read out in parallel from a plurality of light receivers of an image sensor;

a plurality of output control circuits for outputting said plurality of image signals which are processed by said signal processor, to a bus, respectively; and

a data transfer controller for transferring said plurality of image signals output to said bus, wherein

said image sensor functions to output two image signals read out in opposite directions,

said plurality of output control circuits output said two image signals which are processed in parallel by said signal processor, to said bus, respectively, and

said data transfer controller functions to make an order of write addresses of one of said two image signals reverse relative to an order of write addresses of the other of said two image signals.

Claim 16 (Original): The image processing system according to claim 15, wherein

said signal processor also functions to process a plurality of color component signals in parallel which are input in parallel from said image sensor to said signal processor.

Claim 17 (Original): An image capture apparatus comprising:

an image sensor; and

an image processing apparatus for processing an image signal output from said image sensor, wherein

said image processing apparatus comprises:

an input terminal for receiving a plurality of color component signals output in parallel from said image sensor;

a plurality of defective pixel correction circuits for correcting said plurality of color component signals associated with a defective pixel of said image sensor with a predetermined timing; and

a defective pixel correction timing generator for generating said predetermined timing used in performing defective pixel correction at a time of input of said plurality of color component signals, and

said plurality of defective pixel correction circuits of said image processing apparatus correct said plurality of color component signals in parallel at the same time with said predetermined timing, all of said plurality of color component signals being associated with said defective pixel.

Claim 18 (Currently Amended): An image capture apparatus comprising:

an image sensor; and

an image processing apparatus for processing an image signal output from said image sensor, wherein

said image processing apparatus comprises:

[[an]] a plurality of input ~~terminal~~ terminals for receiving a YUV signal and a plurality of color component signals, said YUV signal including a luminance signal and a color difference signal;

a selector for selecting one of said YUV signal and said plurality of color component signals which are input to said selector to provide a selected signal, and outputting said selected signal; and

a signal processor for processing said selected signal, and

one of said input ~~terminal~~ terminals of said image signal processing apparatus is shared by said YUV signal and one of said plurality of color component signals.

Claim 19 (Currently Amended): An image capture apparatus comprising:

an image sensor; and

an image processing system for processing an image signal output from said image sensor, wherein

said image processing system comprises:

a signal processor for processing a plurality of image signals in parallel, including phase adjustment in parallel and defective pixel correction in parallel, which are read out in parallel from a plurality of light receivers of said image sensor;

a plurality of output control circuits for outputting said plurality of image signals which are processed by said signal processor, to a bus, respectively; and

a data transfer controller for transferring said plurality of image signals output to said bus.